

**SYSTEM FOR REDUCING ROW PERIPHERY POWER  
CONSUMPTION IN MEMORY DEVICES**

**ABSTRACT**

The present invention provides a system for reducing row periphery power  
consumption in a semiconductor memory device, particularly during sleep mode operation.  
5 A memory device (100) according to the present invention has a row (106) of memory cells  
and driver circuitry (102) preceding the row of memory cells. The present invention  
provides an intervention circuit (114) instantiated within the driver circuitry proximal to the  
row of memory cells. The intervention circuit is operated to hold the row of memory cells at  
10 a desired state, while the driver circuitry (108, 110) preceding the intervention circuit is  
powered down.